REMARKS

Claims 1-9, 25-26 and 28-31 are all the claims presently pending in the application. Claims 2-3 and 6-7 have been amended to more clearly define the invention. Claims 1, 3, 5-8 and 25 are independent.

Applicant gratefully acknowledges that claims 8 and 25 are allowed, and that claim 30 would be allowable if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Yasumoto, et al. (U.S. Patent No. 4,612,083). Claims 1, 9, 26, 29 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Urushima (J.P. 05-003183), in view of Hayes (U.S. Patent No. 6,114,187). Claims 2 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Urushima, in view of Hayes and in further view of applicants admitted prior art. Claims 3 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art, in view of Capote, et al. (1998 International Symposium on Advanced Packaging Materials). Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art, in view of Hayes.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As discussed during the personal interview, Applicant's invention, as disclosed and recited by, for example, independent claim 1, is directed to a semiconductor device including a stud bump provided on an electrode of the semiconductor chip and an adhesive layer provided on a surface of said semiconductor chip on which the electrode is formed. The stud bump also projects from a surface of the adhesive layer.

The present invention is directed to structures and methods for high density mounting and/or packaging of integrated circuit chips. Conventional mounting systems use interposers to electrically and mechanically connect the semiconductor chip with a substrate onto which the chip is to be mounted.

One conventional method of mounting onto an interposer is known as the flip chip mounting technique (Figs 1A - 1B). A problem with this technique has been the difference in thermal expansion between the semiconductor chip 11 and the interposer 14. To address this issue, an underfill technique has been developed. However, this technique also has problems because the underfill resin 17 does not completely fill the gap between the semiconductor chip and the interposer.

One attempt at solving this problem is illustrated in Figs. 2A - 2B. Bumps 13 are provided on the semiconductor chip 11, a protection film 18 is applied and cured and the cured wafer is polished. This technique is disclosed by the applied Urushima reference (JP No. 5-3183).

While the conventional method illustrated by Figs. 2A - 2B (and the Urushima reference) may alleviate the issue of thermal expansion differences, the mounting of the chip to the interposer is not reliable. In other words, the chip may become separated from the

interposer.

Additionally, mechanical stresses applied to the bumps during mounting may cause damage to the chip.

Another conventional attempt at addressing the problem of different thermal expansion coefficients is illustrated in Fig. 3. This conventional method provides bumps 80 to a semiconductor chip 70 and inserts an adhesive sheet 98 which is manufactured separately. The interposer also includes bumps which will protrude into through holes 102 provided in the adhesive sheet 98 to contact the bumps 80.

However, this conventional method is difficult to perform because accurate control over the position of the adhesive sheet 98 is required in order to ensure that the through holes 102 are accurately placed between the bumps 80 and the connection holes 96. Such accurate arrangement is even more difficult as semiconductor devices become further miniaturized, increase in the number of contacts and bumps become smaller.

Further, since the bumps 80 are not protected before mounting, a load is applied to the bumps during mounting which can cause faulty connections.

By contrast the present invention overcomes all of these problems by providing an adhesive layer on the chip and stud bumps which protrude from the adhesive layer. The adhesive layer on the chip not only serves to protect the stud bumps before and during mounting thereby obviating any need for a protection resin, but also achieves a reliable attachment to the interposer without having to align anything other than the chip with the interposer. Further, the projection of the stud bumps from the adhesive layer adequately ensures reliable transfer of pressing and heating between the electrical contacts to ensure optimal metal junctions.

II. THE PRIOR ART REJECTIONS

A. The Yasumoto et al. reference

Regarding the rejection of claim 7, the Examiner alleges that the Yasumoto et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

As agreed during the personal interview, the Yasumoto et al. reference does not teach or suggest the features of the present invention including stud bumps which project from the adhesive layer. As explained above, this feature is important for ensuring reliable transfer of pressing and heating between the electrical contacts to ensuring optimal metal junctions.

In contrast, the Yasumoto et al. reference discloses stud bumps which are merely exposed at a surface of the adhesive layer (col. 6, lines 21-24). Therefore, the Yasumoto et al. reference does not teach or suggest stud bumps which project from the adhesive layer.

B. The Urushima reference in view of the Hayes reference

Regarding the rejection of claims 1, 9, 26, 29 and 31, the Examiner alleges that the Hayes reference would have been combined with the Urushima reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Urushima reference is directed to overcoming the difficulty of

completely under filling between a mounting substrate and the semiconductor substrate with a protective resin by providing protective resin to the surface of the semiconductor substrate.

In contrast, the Hayes reference is specifically directed to obviating the need for a separate mount (col. 1, line 63 - col. 2, line 4) by printing a package directly onto the integrated circuit (col. 2, lines 5 - 14). In other words, the Hayes reference actually teaches away from providing a separate mount for packaging an IC which is taught by the Urushima reference by actually printing the package directly onto the IC. Thus, one of ordinary skill in the art would not have been motivated to modify the teachings of the Urushima reference with the disclosure of the Hayes reference.

Rather, one of ordinary skill in the art would have been taught to completely abandon the method taught by the Urushima reference and instead to practice the method disclosed by the Hayes reference. Clearly, such an abandonment of the primary purpose of the Urushima reference is contrary to the purpose disclosed by the Urushima reference. Thus, the references would not have been combined, absent hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

The Examiner alleges that one of ordinary skill in the art would have been motivated to modify the teachings of the Urushima reference with stud bumps which project above a dielectric layer "to provide an extended feature which will assure electrical connection to other chips or circuit boards through bonding techniques, such as flip-chip bonding." However, neither of these applied references provide a source for this alleged motivation. The Examiner does not cite any portion of either reference which might provide such a motivation. Applicant respectfully submits that the Examiner does not provide such a

citation because none exists.

Rather, Applicant respectfully submits that the Examiner has engaged in impermissible hindsight. The only reference to such a motivation for providing protruding stud bumps in the file wrapper is found in the specification of the present application. The Examiner cannot use the Applicant's disclosure against the Applicant's claims. Clearly, the Examiner has engaged in the impermissible use of hindsight against the claims of the present application.

As agreed during the personal interview, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention. Neither of the applied references teach or suggest the features of the present invention including an adhesive layer formed on the semiconductor chip. As explained above, this feature is important for protecting the stud bumps before and during mounting thereby obviating any need for a protection resin, but also for achieving a reliable attachment to an interposer without having to align anything other than the chip with the interposer.

Contrary to the Examiner's allegation, the protective layer 12 disclosed by the Urushima reference is not an adhesive layer. Such an allegation is completely baseless. As explained above, the Urushima reference is described in the present specification in detail with reference to Fig. 2. Indeed, the Urushima reference discloses the present inventor's previous invention. The Examiner cannot seriously believe that he is going to contradict the Applicant of the present application when the present Applicant is the author and inventor of the reference being applied against the present claims.

Further, the Examiner's allegation that the protective layer 12 is an adhesive layer

finds absolutely no support in any of the cited documents. Indeed, again as above, the Examiner fails to provide any citation as to where any reference might teach or suggest that the protective layer 12 is an adhesive layer. Applicant respectfully submits that the Examiner does not provide such a citation because no such citation exists. The Examiner has again confused this important distinction between the conventional use of protective films and the present invention which provides multiple advantages over these conventional methods by applying an adhesive layer to the semiconductor chip.

Moreover, the Hayes reference, like the Urushima reference, does not teach or suggest an adhesive layer on the semiconductor chip. As explained above, this feature is important for protecting the stud bumps before and during mounting thereby obviating any need for a protection resin, but also for achieving a reliable attachment to an interposer without having to align anything other than the chip with the interposer.

To the contrary, the Hayes reference discloses forming a dielectric layer 4 on the semiconductor chip from a heated dielectric polymer (col. 6, lines 49-65). The Hayes reference describes the types of polymer which may be used (col. 10, lines 31-40) but does not teach or suggest that the polymer is an adhesive.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1, 9, 26, 29 and 31.

C. The Urushima reference in view of the Hayes reference and Applicant's Admitted Prior Art

Regarding the rejection of claims 2 and 4, the Examiner alleges not only that the Hayes reference would have been combined with the Urushima reference but that the

Applicant's Admitted Prior Art (hereinafter "AAPA") would have been combined with the combination of the Hayes and Urushima references to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

As explained above, clearly one of ordinary skill in the art would not have been motivated to combine the Hayes and Urushima references because they are directed to completely different matters and problems.

The Urushima reference is directed to overcoming the difficulty of completely under filling between a mounting substrate and the semiconductor substrate with a protective resin by providing protective resin to the surface of the semiconductor substrate.

In contrast, the Hayes reference is specifically directed to obviating the need for a separate mount (col. 1, line 63 - col. 2, line 4) by printing a package directly onto the integrated circuit (col. 2, lines 5 - 14). In other words, the Hayes reference actually teaches away from providing a separate mount for packaging an IC which as taught by the Urushima reference by actually printing the package directly onto the IC. Thus, one of ordinary skill in the art would not have been motivated to modify the teachings of the Urushima reference with the disclosure of the Hayes reference.

Rather, one of ordinary skill in the art would have been taught to completely abandon the method taught by the Urushima reference and instead to practice the method disclosed by the Hayes reference. Clearly, such an abandonment of the primary purpose of the Urushima reference is contrary to the purpose disclosed by the Urushima reference. Thus, the Hayes and Urushima references would not have been combined, absent hindsight.

In contrast, Fig. 3 of the AAPA discloses providing an adhesive sheet 98 to bond a

semiconductor chip 70 to the interposer 728. As explained above, the Hayes reference teaches away from using any sort of interposer. Therefore, one of ordinary skill in the art would not have been motivated to modify the teachings of the Hayes reference by providing an adhesive sheet to bond a semiconductor chip to an interposer as disclosed by the AAPA when the Hayes reference teaches completely obviating the need to provide any sort of interposer. Thus, the references would not have been combined, absent hindsight.

As agreed during the personal interview, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the AAPA reference, like the Urushima and Hayes references, does not teach or suggest an adhesive layer formed on the semiconductor chip. As explained above, this feature is important for protecting the stud bumps before and during mounting thereby obviating any need for a protection resin, but also for achieving a reliable attachment to an interposer without having to align anything other than the chip with the interposer.

Clearly, this novel feature is not taught or suggested by the AAPA. The AAPA discloses inserting an adhesive sheet 98 between the semiconductor chip and the interposer. The interposer also includes bumps which will protrude into through holes 102 provided in the adhesive sheet 98 to contact the bumps 80.

However, this conventional method is difficult to perform because accurate control over the position of the adhesive sheet 98 is required in order to ensure that the through holes 102 are accurately placed between the bumps 80 and the connection holes 96. Such accurate arrangement is even more difficult as semiconductor devices become further miniaturized, increase in the number of contacts and bumps become smaller.

Further, since the bumps 80 are not protected before mounting, a load is applied to the

bumps during mounting which can cause faulty connections.

By contrast, the adhesive layer on the semiconductor chip protects the stud bumps before and during mounting thereby obviating any need for a protection resin, and also for achieving a reliable attachment to an interposer without having to align an adhesive sheet.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 2 and 4.

D. The AAPA in view of the Capote et al. reference

Regarding the rejection of claims 3 and 6, the Examiner alleges that the Capote et al. reference would have been combined with the AAPA to form the claimed invention even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Before addressing the subject matter of this rejection, Applicant notes that the Examiner sometimes refers to the Urushima reference and sometimes refers to Figs. 2A - 2B of the AAPA. However, the Examiner need only refer to the Urushima reference because Figs. 2A - 2B of the AAPA is a description of the Urushima reference.

Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, as explained above with regard to the Urushima reference, the AAPA is directed to overcoming the difficulty of completely under filling between a mounting substrate and the semiconductor substrate with a protective resin by providing protective resin to the surface of the semiconductor substrate.

In contrast, the Capote et al. reference is specifically directed to the problem of flux

residue which remains after flux reflow which are generally left in the space between the chip and the substrate. Therefore, one of ordinary skill in the art would not have been motivated to modify the teachings of the AAPA which is directed to overcoming the difficulty of completely under filling with the disclosure of the Capote et al. reference which is concerned with residue flux raising concerns. Thus, the references would not have been combined, absent hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

Even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

As agreed during the personal interview, the AAPA does not teach or suggest an adhesive layer on a surface of the semiconductor chip. As explained above, the adhesive layer is important for protecting the stud bumps before and during mounting thereby obviating any need for a protection resin, but also for achieving a reliable attachment to an interposer without having to align anything other than the chip with the interposer.

Moreover, the Capote et al. reference, like the AAPA, also does not teach or suggest an adhesive layer on a surface of the semiconductor chip. To the contrary, the Capote et al. reference merely discloses a stress distribution layer (i.e. protection resin) on the semiconductor chip. The Capote et al. reference does not teach or suggest an adhesive layer on the semiconductor chip.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims

3 and 6.

E. The AAPA in view of the Hayes reference

Regarding the rejection of claim 5, the Examiner alleges that the Hayes reference would have been combined with the AAPA to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the AAPA is directed to avoiding having to under fill a resin by providing an adhesive sheet 98 to bond a semiconductor chip 70 to the interposer 728.

In contrast, the Hayes reference is specifically directed to obviating the need for a separate mount or interposer (col. 1, line 63 - col. 2, line 4) by printing a package directly onto the integrated circuit (col. 2, lines 5 - 14). In other words, the Hayes reference actually teaches away from providing a separate mount (interposer) for packaging an IC, which as taught by the AAPA, by actually printing the package directly onto the IC. Thus, one of ordinary skill in the art would not have been motivated to modify the teachings of the AAPA with the disclosure of the Hayes reference. Rather, one of ordinary skill in the art would have been taught to completely abandon the method taught by the AAPA and instead to practice the method disclosed by the Hayes reference. Clearly, such an abandonment of the primary purpose of the AAPA is contrary to the purpose disclosed by the AAPA. Thus, these references would not have been combined, absent hindsight.

As agreed during the personal interview, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, neither the AAPA nor the Hayes reference teaches or suggests an adhesive layer formed on the semiconductor chip. As explained above, the adhesive layer formed on the semiconductor chip is important for protecting the stud bumps before and during mounting thereby obviating any need for a protection resin, but also for achieving a reliable attachment to an interposer without having to align anything other than the chip with the interposer.

Clearly, this novel feature is not taught or suggested by the AAPA. The AAPA discloses inserting an adhesive sheet 98 between the semiconductor chip and the interposer. The interposer also includes bumps which will protrude into through holes 102 provided in the adhesive sheet 98 to contact the bumps 80.

However, this conventional method is difficult to perform because accurate control over the position of the adhesive sheet 98 is required in order to ensure that the through holes 102 are accurately placed between the bumps 80 and the connection holes 96. Such accurate arrangement is even more difficult as semiconductor devices become further miniaturized, increase in the number of contacts and bumps become smaller.

Further, since the bumps 80 are not protected before mounting, a load is applied to the bumps during mounting which can cause faulty connections.

By contrast, the adhesive layer on the semiconductor chip protects the stud bumps before and during mounting thereby obviating any need for a protection resin, and also for achieving a reliable attachment to an interposer without having to align an adhesive sheet.

Moreover, the Hayes reference, like the AAPA, does not teach or suggest an adhesive layer on the semiconductor chip. To the contrary, the Hayes reference discloses forming a

dielectric layer 4 on the semiconductor chip from a heated dielectric polymer (col. 6, lines 49-65). The Hayes reference describes the types of polymer which may be used (col. 10, lines 31-40) but does not teach or suggest that the polymer is an adhesive.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claim 5.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-9, 25-26 and 28-31, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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